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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/088,674	06/02/1998	DANIEL J. MORGAN	TI-25995	2025

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EXAMINER	
NGUYEN, KEVIN M	
ART UNIT	**PAPER NUMBER**
2674	28

DATE MAILED: 06/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/088,674	Applicant(s) MORGAN ET AL.	
	Examiner Kevin M. Nguyen	Art Unit 2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The response filed on 04/12/2004 has been fully considered but they are not persuasive. The rejections of claims 1-10 are maintained.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamaguchi et al (US 6,222,515).

As to claims 1 and 6, Yamaguchi et al teaches a system of displaying digital video data associated with a method comprising a logic circuit offsetting a first pixel value a first predetermined amount (2V, 4V) to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount (-2V, -4V) to form a second offset value; and

display panel (19) displaying said first offset pixel value during a first display frame "a positive frame" and displaying said second offset pixel value during a second display frame "a negative frame", such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value "said means

effective voltage of (±3V) is shown by hatching in figure 7B" (see figures 1A, 1B, 7B, column 5, lines 58-64 and column 8, lines 11-27).

As to claims 2 and 7, Yamaguchi et al teaches the system associated the method comprising the value of said first predetermined amount (2V, 4V) is selected by said logic circuit as a function "average" of said first pixel value "said means effective voltage of 3V" (see figures 1A, column 5, lines 58-64).

As to claims 3 and 8, Yamaguchi et al teaches the system associated the method comprising said first offset pixel value (±2V, ±4V) is greater than or less than said first pixel value (3V) as a function "average" of the spatial location that said first pixel value "said means effective voltage of (±3V)" is to be displayed (see figures 1A, 7B, column 8, lines 11-27).

As to claims 4 and 9, Yamaguchi et al teaches the system associated with the method comprising said pixel value are displayed using a plurality of weighted bit-planes "a first field memory (13), a second field memory (14)", wherein said first pixel values close to a bit transition of said bit-planes (13, 14) are offset during said first display frame "said positive frame" and said second frame "said negative frame" (see figure 1B, column 6, lines 41-55).

As to claims 5 and 10, Yamaguchi et al teaches the system associated with the method comprising said first display frame "said positive frame and said second display frame "said negative frame" are consecutive (see figure 7B, column 8, lines 11-27).

Response to Arguments

4. Applicant's arguments filed 04/12/2004 have been fully considered but they are not persuasive.

5. In response to applicant's argument that claim 1 recites "offsetting a first pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and offset said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value."

This argument is not persuasive because Yamaguchi et al teaches "to realize a gray scale level 3, 6 (V) an applied to the first field and 2 (V) to the second field (fig. 7, col. 8, lines 23-24). An image of one frame is written in the first and second field frame memories 13 and 14 (col. 8, line 11-12). This means effective voltage is shown by hatching in figs. 7A to 7D (col. 8, lines 18-19). Accordingly, the teaching of Yamaguchi meets the claimed limitation recited in lines 3-5 of claim 1.

Here, the voltage levels for realizing the gray-scale level 1 in a positive frame are equal to those for realizing the gray-scale level 4 in a negative frame. Similarly, the voltage levels for realizing the gray-scale level 2 in a positive frame are equal to those for realizing the gray scale level 3 in a negative frame (fig 17, col. 10, lines 8-15). Accordingly, the teaching of Yamaguchi meets the claimed limitation recited in lines 6-8 of claim 1.

Realizing a gray scale level 3, 6 (V) an applied to the first field and 2 (V) to the second field to produce a mean effective voltage of 4 (V) for one frame (fig. 7, col. 8, lines 23-25). Accordingly, the teaching of Yamaguchi meets the claimed limitation "average of said displayed first offset pixel value 6 (V) and said second offset pixel value 2 (V) is said first pixel value (a mean effective voltage of 4 (V))".

6. In response to applicant's argument that claim 6 recites "a logic circuit offsetting a first pixel value a first predetermined amount to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value; and display means displaying said first offset pixel value during a first display frame and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value."

This argument is not persuasive because Yamaguchi et al teaches this embodiment is an example that realizes four gray-scale levels using a data driver for two gray-scale levels. The pixel selecting part 2 involves a scan driver 7, and data drivers 8. The data signal generating part 3 involves an A/D conversion portion 9, a data conversion portion 10, a first parallel conversion portion 11, a second parallel conversion portion 12, a first-field frame memory 13, a second-field frame memory 14, and a display data switching portion 15. The voltage applying part 4 involves a first-frame liquid crystal driving source 16 serving as a voltage applying portion, a second-frame liquid crystal driving source 17 serving as the voltage applying portion, a driving

source switching portion 18, and a common voltage source portion 21. The liquid crystal display part 5 involves a liquid crystal display panel 19 (figs. 1A, 1B, col. 5, lines 50-64).

Accordingly, said data drivers 8 (fig. 1B), said scan driver 7 (fig. 1B), said first field frame memory 13 (fig. 1B), said second field frame memory 14 (fig. 1B), said LCD driving source for first field V1, V2, V3, V4 (16) (fig. 1A), said LCD driving source for second filed V1, V2, V3, V4 (17) (fig. 1A), and RGB signal (fig. 1A) correspond to the logic circuit as claimed. Said liquid crystal display part 5 corresponds to the display means as claimed. The operation of these devices illustrated in paragraphs 5 above.

For these reasons, the rejections based on Yamaguchi et al have been maintained.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on MON-THU from 9:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reached on **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Patent Examiner
Art Unit 2674

KN
June 9, 2004

XIAO WU
PRIMARY EXAMINER